stantial current, especially compared to HC and HCT output capabilities. For example, an HC or HCT output can drive 10 LS or only two S-TTL inputs.

The last factor is capacitive loading. We've seen that load capacitance increases both the delay and the power dissipation of logic circuits. Increases in delay are especially noticeable with HC and HCT outputs, whose transition times increase about 1 ns for each 5 pF of load capacitance. The transistors in FCT outputs have very low "on" resistances, so their transition times increase only about 0.1 ns for each 5 pF of load capacitance.

For a given load capacitance, power-supply voltage, and application, all of the CMOS families have similar dynamic power dissipation, since each variable in the CV^2f equation is the same. On the other hand, TTL outputs have somewhat lower dynamic power dissipation, since the voltage swing between TTL HIGH and LOW levels is smaller.

*3.13 Low-Voltage CMOS Logic and Interfacing

Two important factors have led the IC industry to move towards lower power-supply voltages in CMOS devices:

- In most applications, CMOS output voltages swing from rail to rail, so the V in the CV^2f equation is the power-supply voltage. Cutting power-supply voltage reduces dynamic power dissipation more than proportionally.
- As the industry moves towards ever-smaller transistor geometries, the oxide insulation between a CMOS transistor's gate and its source and drain is getting ever thinner, and thus incapable of insulating voltage potentials as "high" as 5 V.

As a result, JEDEC, an IC industry standards group, selected $3.3\,V \pm 0.3V$, $2.5\,V \pm 0.2V$, and $1.8\,V \pm 0.15V$ as the next "standard" logic power-supply voltages. JEDEC standards specify the input and output logic voltage levels for devices operating with these power-supply voltages.

The migration to lower voltages has occurred in stages, and will continue to do so. For discrete logic families, the trend has been to produce parts that operate and produce outputs at the lower voltage, but that can also tolerate inputs at the higher voltage. This approach has allowed 3.3-V CMOS families to operate with 5-V CMOS and TTL families, as we'll see in the next section.

Many ASICs and microprocessors have followed a similar approach, but another approach is often used as well. These devices are large enough that it can make sense to provide them with two power-supply voltages. A low voltage, such as 2.5 V, is supplied to operate the chip's internal gates, or *core logic*. A higher voltage, such as 3.3 V, is supplied to operate the external input and output circuits, or *pad ring*, for compatibility with older-generation devices in the system. Special buffer circuits are used internally to translate safely and quickly between the core-logic and the pad-ring logic voltages.

core logic

pad ring

*3.13.1 3.3-V LVTTL and LVCMOS Logic

The relationships among signal levels for standard TTL and low-voltage CMOS devices operating at their nominal power-supply voltages are illustrated nicely in Figure 3-85, adapted from a Texas Instruments application note. The original, symmetric signal levels for pure 5-V CMOS families such as HC and VHC are shown in (a). TTL-compatible CMOS families such as HCT, VHCT, and FCT shift the voltage levels downwards for compatibility with TTL as shown in (b).

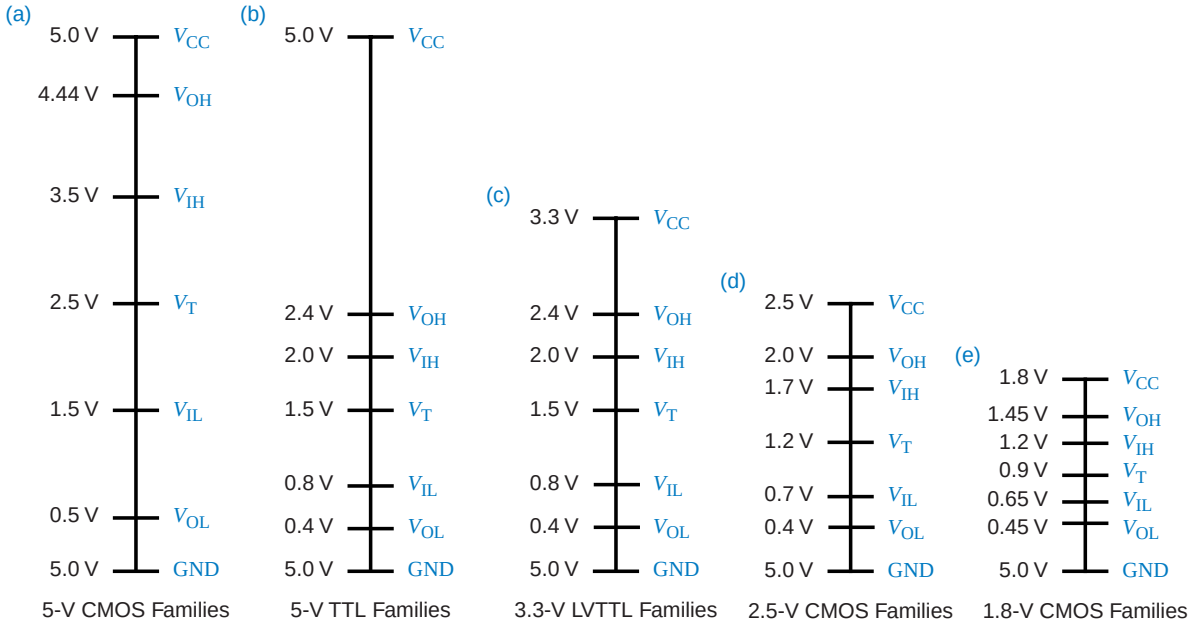
LVCMOS (low-voltage CMOS)

LVTTL (low-voltage TTL)

The first step in the progression of lower CMOS power-supply voltages was 3.3 V. The JEDEC standard for 3.3-V logic actually defines two sets of levels. *LVCMOS (low-voltage CMOS)* levels are used in pure CMOS applications where outputs have light DC loads (less than 100 μA), so V_{OL} and V_{OH} are maintained within 0.2 V of the power-supply rails. *LVTTL (low-voltage TTL)* levels, shown in (c), are used in applications where outputs have significant DC loads, so V_{OL} can be as high as 0.4 V and V_{OH} can be as low as 2.4 V.

The positioning of TTL's logic levels at the low end of the 5-V range was really quite fortuitous. As shown in Figure 3-85(b) and (c), it was possible to define the LVTTL levels to match up with TTL levels exactly. Thus, an LVTTL output can drive a TTL input with no problem, as long as its output current specifications (I_{OLmax}, I_{OHmax}) are respected. Similarly, a TTL output can drive an LVTTL input, except for the problem of driving it beyond LVTTL's 3.3-V V_{CC}, as discussed next.

Figure 3-85 Comparison of logic levels: (a) 5-V CMOS; (b) 5-V TTL, including 5-V TTL-compatible CMOS; (c) 3.3-V LVTTL; (d) 2.5-V CMOS; (e) 1.8-V CMOS.



*3.13.2 5-V Tolerant Inputs

The inputs of a gate won't necessarily tolerate voltages greater than V_{CC}. This can easily occur when 5-V and 3.3-V logic families in a system. For example, 5-V CMOS devices easily produce 4.9-V outputs when lightly loaded, and both CMOS and TTL devices routinely produce 4.0-V outputs even when moderately loaded.

The maximum voltage V_{Imax} that can be tolerated by an input is listed in the "absolute maximum ratings" section of the manufacturer's data sheet. For HC devices, V_{Imax} equals V_{CC}. Thus, if an HC device is powered by a 3.3-V supply, its cannot be driven by any 5-V CMOS or TTL outputs. For VHC devices, on the other hand, V_{Imax} is 7 V; thus, VHC devices with a 3.3-V power supply may be used to convert 5-V outputs to 3.3-V levels for use with 3.3-V microprocessors, memories, and other devices in a pure 3.3-V subsystem.

Figure 3-86 explains why some inputs are 5-V tolerant and others are not. As shown in (a), the HC and HCT input structure actually contains two reverse-biased *clamp diodes*, which we haven't shown before, between each input signal and V_{CC} and ground. The purpose of these diodes is specifically to shunt any transient input signal value less than 0 through *D1* or greater than V_{CC} through *D2* to the corresponding power-supply rail. Such transients can occur as a result of transmission-line reflections, as described in Section 12.4. Shunting the so-called "undershoot" or "overshoot" to ground or V_{CC} reduces the magnitude and duration of reflections.

clamp diode

Of course, diode *D2* can't distinguish between transient overshoot and a persistent input voltage greater than V_{CC}. Hence, if a 5-V output is connected to one of these inputs, it will not see the very high impedance normally associated with a CMOS input. Instead, it will see a relatively low impedance path to V_{CC} through the now forward-biased diode *D2*, and excessive current will flow.

Figure 3-86(b) shows a 5-V tolerant CMOS input. This input structure simply omits *D2*; diode *D1* is still provided to clamp undershoot. The VHC and AHC families use this input structure.

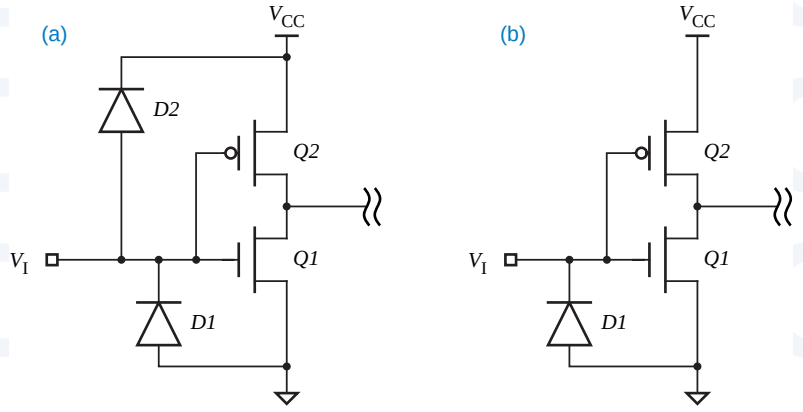


Figure 3-86
CMOS input structures: (a) non-5-V tolerant HC; (b) 5-V tolerant VHC.

The kind of input structure shown in Figure 3-86(b) is necessary but not sufficient to create 5-V tolerant inputs. The transistors in a device's particular fabrication process must also be able to withstand voltage potentials higher than V_{CC}. On this basis, V_{Imax} in the VHC family is limited to 7.0 V. In many 3.3-V ASIC processes, it's not possible to get 5-V tolerant inputs, even if you're willing to give up the transmission-line benefits of diode *D2*.

*3.13.3 5-V Tolerant Outputs

Five-volt tolerance must also be considered for outputs, in particular, when both 3.3-V and 5-V three-state outputs are connected to a bus. When the 3.3-V output is in the disabled, Hi-Z state, a 5-V device may be driving the bus, and a 5-V signal may appear on the 3.3-V device's *output*.

In this situation, Figure 3-87 explains why some outputs are 5-V tolerant and others are not. As shown in (a), the standard CMOS three-state output has an *n*-channel transistor *Q1* to ground and a *p*-channel transistor *Q2* to V_{CC}. When the output is disabled, circuitry (not shown) holds the gate of *Q1* near 0 V, and the gate of *Q2* near V_{CC}, so both transistors are off and Y is Hi-Z.

Now consider what happens if V_{CC} is 3.3 V and a different device applies a 5-V signal to the output pin Y in (a). Then the drain of *Q2* (Y) is at 5 V while the gate (V_2) is still at only 3.3 V. With the gate at a lower potential than the drain, *Q2* will begin to conduct and provide a relatively low-impedance path from Y to V_{CC}, and excessive current will flow. Both HC and VHC three-state outputs have this structure and therefore are not 5-V tolerant.

Figure 3-87(b) shows a 5-V tolerant output structure. An extra *p*-channel transistor *Q3* is used to prevent *Q2* from turning on when it shouldn't. When V_{OUT} is greater than V_{CC}, *Q3* turns on. This forms a relatively low impedance path from Y to the gate of *Q2*, which now stays off because its gate voltage V_2 can no longer be below the drain voltage. This output structure is used in Texas Instruments' LVC (Low-Voltage CMOS) family.

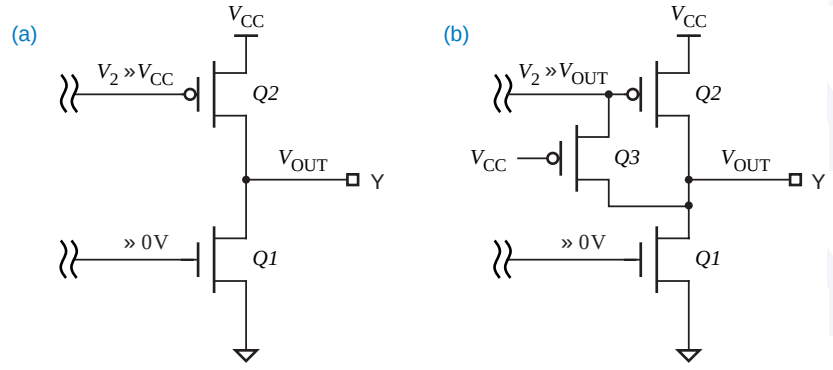


Figure 3-87
CMOS three-state output structures: (a) non-5-V tolerant HC and VHC; b) 5-V tolerant LVC.

*3.13.4 TTL/LVTTL Interfacing Summary

Based on the information in the preceding subsections, TTL (5-V) and LVTTL (3.3-V) devices can be mixed in the same system subject to just three rules:

1. LVTTL outputs can drive TTL inputs directly, subject to the usual constraints on output current (I_{OLmax}, I_{OHmax}) of the driving devices.
2. TTL outputs can drive LVTTL inputs if the inputs are 5-V tolerant.
3. TTL and LVTTL three-state outputs can drive the same bus if the LVTTL outputs are 5-V tolerant.

*3.13.5 2.5-V and 1.8-V Logic

The transition from 3.3-V to 2.5-V logic will not be so easy. It is true that 3.3-V outputs can drive 2.5-V inputs as long as the inputs are 3.3-V tolerant. However, a quick look at Figure 3-85(c) and (d) on page 168 shows that V_{OH} of a 2.5-V output equals V_{IH} of a 3.3-V input. In other words, there is zero HIGH-state DC noise margin when a 2.5-V output drives a 3.3-V input, not a good situation.

level translator
level shifter

The solution to this problem is to use a *level translator or level shifter*, a device which is powered by both supply voltages and which internally boosts the lower logic levels (2.5 V) to the higher ones (3.3 V). Many of today's ASICs and microprocessors contain level translators internally, allowing them to operate with a 2.5-V or 2.7-V core and a 3.3-V pad ring, as we discussed at the beginning of this section. If and when 2.5-V discrete devices become popular, we can expect the major semiconductor vendors produce level translators as stand-alone components as well.

The next step will be a transition from 2.5-V to 1.8-V logic. Referring to Figure 3-85(d) and (e), you can see that the HIGH-state DC noise margin is actually negative when a 1.8-V output drives a 2.5-V input, so level translators will be needed in this case also.

*3.14 Emitter-Coupled Logic

The key to reducing propagation delay in a bipolar logic family is to prevent a gate's transistors from saturating. In Section 3.9.5, we learned how Schottky diodes prevent saturation in TTL gates. However, it is also possible to prevent saturation by using a radically different circuit structure, called *current-mode logic (CML)* or *emitter-coupled logic (ECL)*.

current-mode logic (CML)

Unlike the other logic families in this chapter, CML does not produce a large voltage swing between the LOW and HIGH levels. Instead, it has a small voltage swing, less than a volt, and it internally switches current between two possible paths, depending on the output state.

emitter-coupled logic (ECL)

The first CML logic family was introduced by General Electric in 1961. The concept was soon refined by Motorola and others to produce the still popular 10K and 100K *emitter-coupled logic (ECL)* families. These families are

emitter-coupled logic (ECL)