*3.14.3 ECL 100K Family

ECL 100K family

Members of the *ECL 100K family* have 6-digit part numbers of the form "100xxx" (e.g., 100101, 100117, 100170), but in general have functions different than 10K parts with similar numbers. The 100K family has the following major differences from the 10K family:

- Reduced power-supply voltage, $V_{EE} = -4.5$ V.
- Different logic levels, as a consequence of the different supply voltage.
- Shorter propagation delays, typically 0.75 ns.
- Shorter transition times, typically 0.70 ns.
- Higher power consumption, typically 40 mW per gate.

*3.14.4 Positive ECL (PECL)

We described the advantage of noise immunity provided by ECL's negative power supply ($V_{EE} = -5.2$ V or -4.5 V), but there's also a big disadvantage—today's most popular CMOS and TTL logic families, ASICs, and microprocessors all use a positive power-supply voltage, typically +5.0 V but trending to +3.3 V. Systems incorporating both ECL and CMOS/TTL devices therefore require two power supplies. In addition, interfacing between standard, negative ECL 10K or 100K logic levels and positive CMOS/TTL levels requires special level-translation components that connect to both supplies.

positive ECL (PECL)

Positive ECL (*PECL*, pronounced "peckle") uses a standard +5.0-V power supply. Note that there's nothing in the ECL 10K circuit design of Figure 3-92 that requires V_{CC} to be grounded and V_{EE} to be connected to a -5.2-V supply. The circuit will function exactly the same with V_{EE} connected to ground, and V_{CC} to a +5.2-V supply.

Thus, PECL components are nothing more than standard ECL components with V_{EE} connected to ground and V_{CC} to a +5.0-V supply. The voltage between V_{EE} and V_{CC} is a little less than with standard 10K ECL and more than with standard 100K ECL, but the 10H-series and 100K parts are voltage compensated, designed to still work well with the supply voltage being a little high or low.

Like ECL logic levels, PECL levels are referenced to V_{CC}, so the PECL HIGH level is about $V_{CC} - 0.9$ V, and LOW is about $V_{CC} - 1.7$ V, or about 4.1 V and 3.3 V with a nominal 5-V V_{CC}. Since these levels are referenced to V_{CC}, they move up and down with any variations in V_{CC}. Thus, PECL designs require particularly close attention to power distribution issues, to prevent noise on V_{CC} from corrupting the logic levels transmitted and received by PECL devices.

Recall that CML/ECL devices produce differential outputs and can have differential inputs. A differential input is relatively insensitive to the absolute voltage levels of an input-signal pair, and only to their difference. Therefore, differential signals can be used quite effectively in PECL applications to ease the noise concerns raised in the preceding paragraph.

It is also quite common to provide differential PECL-compatible inputs and outputs on CMOS devices, allowing a direct interface between the CMOS device and a device such as a fiber-optic transceiver that expects ECL or PECL levels. In fact, as CMOS circuits have migrated to 3.3-V power supplies, it has even been possible to build PECL-like differential inputs and outputs that are simple referenced to the 3.3-V supply instead of a 5-V supply.

References

Students who need to study the basics may wish to consult "Electrical Circuits Review" by Bruce M. Fleischer. This 20-page tutorial covers all of the basic circuit concepts that are used in this chapter. It appears both as an appendix in this book's first edition and as a PDF file on its web page, www.ddpp.com.

If you're interested in history, a nice introduction to all of the early bipolar logic families can be found in *Logic Design with Integrated Circuits* by William E. Wickes (Wiley-Interscience, 1968). The classic introduction to TTL electrical characteristics appeared in *The TTL Applications Handbook*, edited by Peter Alfke and Ib Larsen (Fairchild Semiconductor, 1973). Early logic designers also enjoyed *The TTL Cookbook* by Don Lancaster.

For another perspective on the electronics material in this chapter, you can consult almost any modern electronics text. Many contain a much more analytical discussion of digital circuit operation; for example, see *Microelectronics* by J. Millman and A. Grabel (McGraw-Hill, 1987, 2nd ed.). Another good introduction to ICs and important logic families can be found in *VLSI System Design* by Saburo Muroga (Wiley, 1982). For NMOS and CMOS circuits in particular, two good books are *Introduction to VLSI Systems* by Carver Mead and Lynn Conway (Addison-Wesley, 1980) and *Principles of CMOS VLSI Design* by Neil H. E. Weste and Kamran Eshraghian (Addison-Wesley, 1993).

Characteristics of today's logic families can be found in the data books published by the device manufacturers. Both Texas Instruments and Motorola publish comprehensive data books for TTL and CMOS devices, as listed in Table 3-13. Both manufacturers keep up-to-date versions of their data books on the web, at www.ti.com and www.mot.com. Motorola also provides a nice introduction to ECL design in their *MECL System Design Handbook* (publ. HB205, rev. 1, 1988).

Howie Johnson?

BeeBop?

The JEDEC standards for digital logic levels can be found on JEDEC's web site, www.jedec.org. (Joint Electron Device Engineering Council). The JEDEC standards for 3.3-V, 2.5-V, and 1.8-V logic were published in 1994, 1995, and 1997, respectively.