3e3.3 3.3 A logic buffer is a non-linear amplifier that maps the entire set of possible analog input voltages into just two output votages, HIGH and LOW. An audio amplifier has a linear response over its specified operating range, mapping each input voltage into an output voltage that is directly proprtional to the input voltage.

3e3.6 3.6 From the *American Heritage Electronic Dictionary (AHED)*, copyright 1992 by Houghton Mifflin Company:

(1) A structure that can be swung, drawn, or lowered to block an entrance or a passageway.

(2) a. An opening in a wall or fence for entrance or exit. b. The structure surrounding such an opening, such as the monumental or fortified entrance to a palace or walled city.

(3) a. A means of access: the gate to riches. b. A passageway, as in an airport terminal, through which passengers proceed for embarkation.

(4) A mountain pass.

(5) The total paid attendance or admission receipts at a public event: a good gate at the football game.

(6) A device for controlling the passage of water or gas through a dam or conduit.

(7) The channel through which molten metal flows into a shaped cavity of a mold.

(8) Sports. A passage between two upright poles through which a skier must go in a slalom race.

(9) Electronics. A circuit with multiple inputs and one output that is energized only when a designated set of input pulses is received.

Well, definition (9) is closest to one of the answers that I had in mind. The other answer I was looking for is the gate of a MOS transistor.

3e3.14 3.16 A CMOS inverting gate has fewer transistors than a noninverting one, since an inversion comes "for free."

3e3.18 3.19 One way is that a romance could be sparked, and the designers could end up with a lot less time to do their work. Another way is that the stray perfume in the IC production line could have contaminated the circuits used by the designers, leading to marginal operation, more debugging time by the deidicated designers, and less time for romance. By the way, the whole perfume story may be apocryphal.

3e3.20 3.20 Using the maximum output current ratings in both states, the HIGH-state margin is 0.69 V and the LOW-state margin is 1.02 V. With CMOS loads (output currents less than 20 μA), the margins improve to 1.349 V and 1.25 V, respectively.

3e3.21 3.22 The first answer for each parameter below assumes commercial operation and that the device is used with the maximum allowable (TTL) load. The number in parentheses, if any, indicates the value obtained under a lesser but specified (CMOS) load.

V_{OHmin}	3.84 V (4.4 V)
V_{IHmin}	3.15 V
V_{ILmax}	1.35 V
V_{OLmax}	0.33 V (0.1 V)
I_{Imax}	1 μA
I_{OLmax}	4 mA (20 μA)
I_{OHmax}	-4 mA (-20 μA)

3e3.24 3.24 (Note typo in the first printing; change "2.0–5.0 V" to "3.15–5.0 V.") The specification for the 74HC00 shows a maximum power-supply current of 10 μA when the inputs are at 0 or 5 V, but based on the discussion in Section 3.5.3 we would expect the current to be more when the inputs are at their worst-case values (1.35 or 3.15 V). If we consider "nonlogic" input values, the maximum current will flow if the inputs are held right at the switching threshold, approximately $V_{CC}/2$.

3e3.26 3.26 Using the formulas on page 120, we can estimate that $R_{p(on)} = (5.0 - 3.84)/0.004 = 290\Omega$ or, using the higher value of V_{OHmin} in the spec, that $R_{p(on)} = (5.0 - 4.4)/0.00002 = 30\text{K}\Omega$. (The discrepancy shows that the output characteristic of this device is somewhat nonlinear.) We can also estimate $R_{n(on)} = 0.33/0.004 = 82.5\Omega$.

3e3.38 3.39 Smaller resistors result in shorter rise times for LOW-to-HIGH transitions but higher power consumption in the LOW state. Stated another way, larger resistors result in lower power consumption in the LOW state but longer rise times (more ooze) for LOW -to-HIGH transitions.

3e3.41 3.42 The wired output has only passive pull-up to the HIGH state. Therefore, the time for LOW-to-HIGH transitions, an important component of total delay, depends on the amount of capacitive loading and the size of the pull-up resistor. A moderate capacitive load (say, 100 pF) and even a very strong pull-up resistor (say, 150Ω) can still lead to time constants and transition times (15 ns in this example) that are longer than the delay of an additional gate with active pull-up.

3e3.42 3.43 The winner is 74FCT-T—48 mA in the LOW state and 15 mA in the HIGH state (see Table 3–8). TTL families don't come close.

3e3.46 3.47 n diodes are required.

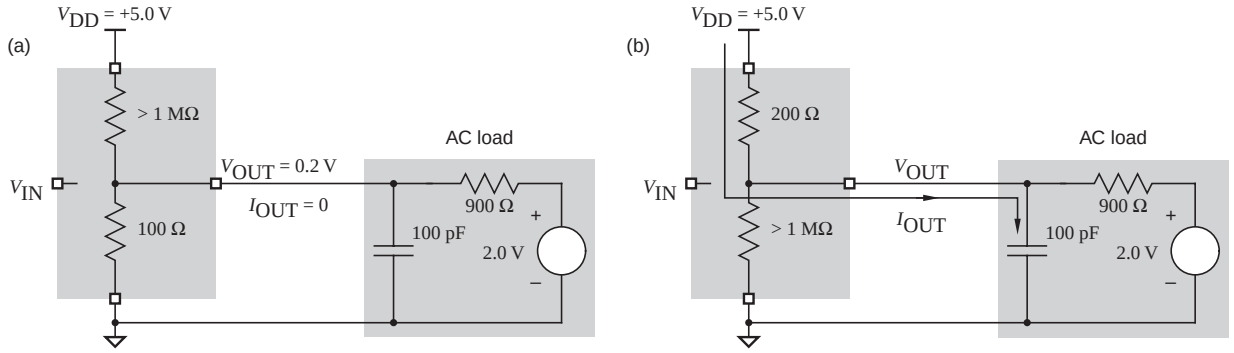
3.50 LS-TTL output driving the input. Since $I_{\text{ILmax}} = 0.4\text{mA}$, we get $R_{\text{pd}} = 0.5/0.004 = 1250\Omega$ and $P_{pd} = V_{\text{IL}}^2/R_{\text{pd}} = (0.5)^2/1250 = 0.2\text{mW}$. (Alternatively, $P_{\text{pd}} = V_{\text{IL}}I_{\text{IL}} = 0.5 \cdot 0.0004 = 0.2\text{mW}$)

For the pull-up, we must have at most a 2.3-V drop in order to create a V_{IH} that is no worse than a standard LS-TTL output driving the input. Since $I_{\text{IHmax}} = 20\mu\text{A}$, we get $R_{\text{pu}} = 2.3/0.00002 = 115\text{k}\Omega$ and $P_{\text{pu}} = V_{\text{IH}}^2/R_{\text{pu}} = (2.3)^2/115000 = 0.046\text{mW}$. (Alternatively, we could have calculated the result as $P_{\text{pu}} = V_{\text{IH}}I_{\text{IH}} = 2.3 \cdot 0.00002 = 0.046\text{mW}$.) The pull-up dissipates less power.

3e3.52 3.52 The main benefit of Schottky diodes is to prevent transistors from saturating, which allows them to switch more quickly. The main drawback is that they raise the collector-to-emitter drop across an almost-saturated transistor, which decreases LOW -state noise margin.

3e3.64 3.64 TTL-compatible inputs have $V_{\text{IHmin}} = 2.0\text{V}$, and typical TTL outputs have $V_{\text{OHmin}} = 2.7\text{V}$. CMOS output levels are already high compared to these levels, so there's no point in wasting silicon to make them any higher by lowering the voltage drop in the HIGH state.

3e3.69 **3.69** Rise time can be calculated in a manner similar to the solution of Exercise 3.68. Part (a) of the figure below shows the conditions in the circuit when the output is in a steady LOW state with $V_{OUT} = 0.2\,V$ as predicted in Exercise 3.68. If at time $t = 0$ the CMOS output changes to the HIGH state, the situation depicted in (b) results. The Thévenin equivalent of the voltage source and the two resistors in the HIGH state is 163.6Ω in series with a 4.545-V voltage source.



V_{OUT} cannot change instantly, but at time $t = \infty$, the capacitor will be charged to the Thévenin -equivalent voltage of $4.545\,V$. Until then, the value of V_{OUT} in between is governed by an exponential law:

$$\begin{aligned} V_{OUT} &= 0.2V + (4.545 - 0.2V) \cdot (1 - e^{-t/R_p C_L}) \\ &= 0.2V + 4.345 \cdot (1 - e^{-t/163.6 \cdot 100 \cdot 10^{-12}})V \\ &= 0.2V + 4.345 \cdot (1 - e^{-t/16.36 \cdot 10^{-9}})V \end{aligned}$$

The *RC* time constant in this case is 16.36 ns. To obtain the rise time, we must solve the preceding equation for $V_{OUT} = 1.5$ and $V_{OUT} = 3.5$, yielding

$$t = -16.36 \cdot 10^{-9} \cdot \ln\frac{4.545 - V_{OUT}}{4.356}$$

$$t_{1.5} = 5.82 \text{ ns}$$

$$t_{3.5} = 23.35 \text{ ns}$$

The rise time t_r is the difference between these two numbers, or 17.53 ns. Although the time constant is shorter than in Section 3.6.1, the asymptote of 4.545 V is appreciably closer to the threshold than the 5-V asymptote in Section 3.6.1, so the rising edge starts slowing sooner, and the overall rise time is slightly longer than the 17-ns result in Section 3.6.1 (as suggested in the solution to Exercise 3.67).

3e3.70 **3.70** The time constant is $1k\Omega \cdot 50\text{ pF} = 50\text{ ns}$. We solve the rise-time equation for the point at which V_{OUT} is 1.5 V, as on p. 119 of the text:

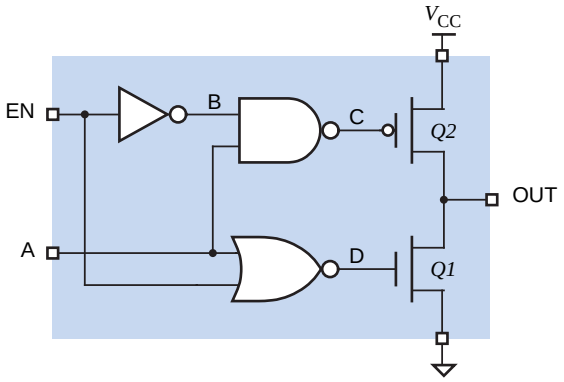
$$t_{1.5} = -50 \cdot 10^{-9} \cdot \ln\frac{5.0 - 1.5}{5.0}$$

$$t_{1.5} = 17.83 \text{ ns}$$

3e3.77 **3.79** The LSB toggles at a rate of 16 MHz. It takes two clock ticks for the LSB to complete one cycle, so the transition frequency is 8 MHz. The MSB's frequency is 2^7 times slower, or 62.5 KHz. The LSB's dynamic power is the most significant, but the sum of the transitions on the higher order bits, a binary series, is equivalent to almost another 8 MHz worth of transitions on a single output bit. Including the LSB, we have almost 16 MHz, but applied to the load capacitance on just a single output. If the different ouputs actually have different load capacitances, then a weighted average would have to be used.

3e3.81 3.83

(a)



(b)

EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	H	on	off	L
L	H	H	L	L	off	on	H
H	L	L	H	L	off	off	Hi-Z
H	H	L	H	L	off	off	Hi-Z

(c)