BiPLD: Bipolar PLD Circuits

BiPLD.1 Circuit Structure

There are several different circuit technologies for building and physically programming a PLD. Early commercial PLAs and PAL devices used bipolar circuits. For example, Figure BiPLD-1 shows how the example 4 × 3 PLA circuit of the preceding section might be built in a bipolar, TTL-like technology. Each potential connection is made by a diode in series with a metal link that may be present or absent. If the link is present, then the diode connects its input into a diode-AND function. If the link is missing, then the corresponding input has no effect on that AND function.

A diode-AND function is performed because each and every horizontal "input" line that is connected via a diode to a particular vertical "AND" line must be HIGH in order for that AND line to be HIGH. If an input line is LOW, it pulls LOW all of the AND lines to which it is connected. This first matrix of circuit elements that perform the AND function is called the *AND plane*.

AND plane

Each AND line is followed by an inverting buffer, so overall a NAND function is obtained. The outputs of the first-level NAND functions are combined by another set of programmable diode AND functions, once again followed by inverters. The result is a two-level NAND-NAND structure that is functionally equivalent to the AND-OR PLA structure described in the preceding section. The matrix of circuit elements that perform the OR function (or the second NAND function, depending on how you look at it) is called the *OR plane*.

OR plane

A bipolar PLD chip is manufactured with all of its diodes present, but with a tiny *fusible link* in series with each one (the squiggles in Figure BiPLD-1). By applying special input patterns to the device, it is possible to select individual links, apply a high voltage (10–30 V), and thereby vaporize selected links.

fusible link

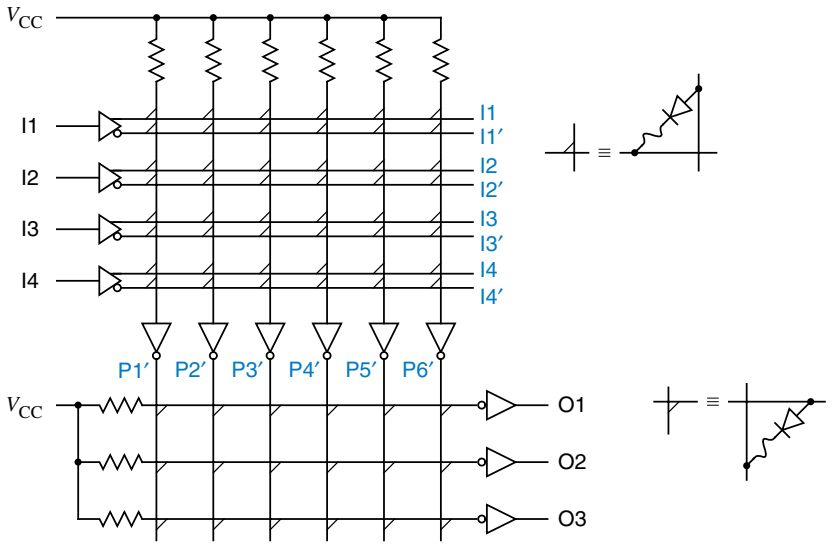

Figure BiPLD-1
A 4 × 3 PLA built using TTL-like open-collector gates and diode logic.

Early bipolar PLDs had reliability problems. Sometimes the stored patterns changed because of incompletely vaporized links that would "grow back," and sometimes intermittent failures occurred because of floating shrapnel inside the IC package. However, these problems have been largely worked out, and reliable fusible-link technology is used in today's bipolar PLDs.

BiPLD.2 Bipolar Sequential PLDs

PAL16R8

The *PAL16R8*, shown in Figure BiPLD-2, is representative of the first generation of sequential PLDs, which used bipolar (TTL) technology. This device has eight primary inputs, eight outputs, and common clock and output-enable inputs, and it fits in a 20-pin package.

The PAL16R8's AND-OR array is exactly the same as the one found in the PAL16L8 combinational PLD. However, the PAL16R8 has edge-triggered D flip-flops between the AND-OR array and its eight outputs, O1–O8. All of the flip-flops are connected to a common clock input, CLK, and change state on the rising edge of the clock. Each flip-flop drives an output pin through a three-state buffer; the buffers have a common output-enable signal, OE_L. Notice that, like the combinational output pins of a PAL16L8, the registered output pins of the PAL16R8 contain the complement of the signal produced by the AND-OR array.

The possible inputs to the PAL16R8's AND-OR array are eight primary inputs (I1–I8) and the outputs of eight D flip-flops. The connection from the D-flip-flop outputs into the AND-OR array makes it easy to design shift registers, counters, and general state machines. Unlike the PAL16L8's combinational outputs, the PAL16R8's D-flip-flop outputs are available to the AND-OR array whether or not the O1–O8 three-state drivers are enabled. Thus, the internal flip-flops can go to a next state that is a function of the current state even when the O1–O8 outputs are disabled.

Many applications require combinational as well as sequential PLD outputs. The manufacturers of bipolar PLDs addressed this need by providing a few variants of the PAL16R8 that omitted the D flip-flops on some output pins, and instead provided input and output capability identical to that of the PAL16L8's bidirectional pins. For example, Figure BiPLD-3 is the logic diagram of the *PAL16R6*, which has only six registered outputs. Two pins, IO1 and IO8, are bidirectional, serving both as inputs and as combinational outputs with separate three-state enables, just like the PAL16L8's bidirectional pins. Thus, the possible inputs to the PAL16R6's AND-OR array are the eight primary inputs (I1–I8), the six D-flip-flop outputs, and the two bidirectional pins (IO1, IO8).

PAL16R6

PAL16L8

Table BiPLD-1 shows eight standard bipolar PLDs with differing numbers and types of inputs and outputs. All of the PAL16xx parts in the table use the same AND-OR array, where each output has eight AND gates, each with 16 variables and their complements as possible inputs. The PAL20xx parts use a similar AND-OR array with 20 variables and their complements as possible inputs. Figure BiPLD-4 shows logic symbols for all of the PLDs in the table.

PAL16R4
PAL16R8
PAL20L8
PAL20R4
PAL20R6
PAL20R8

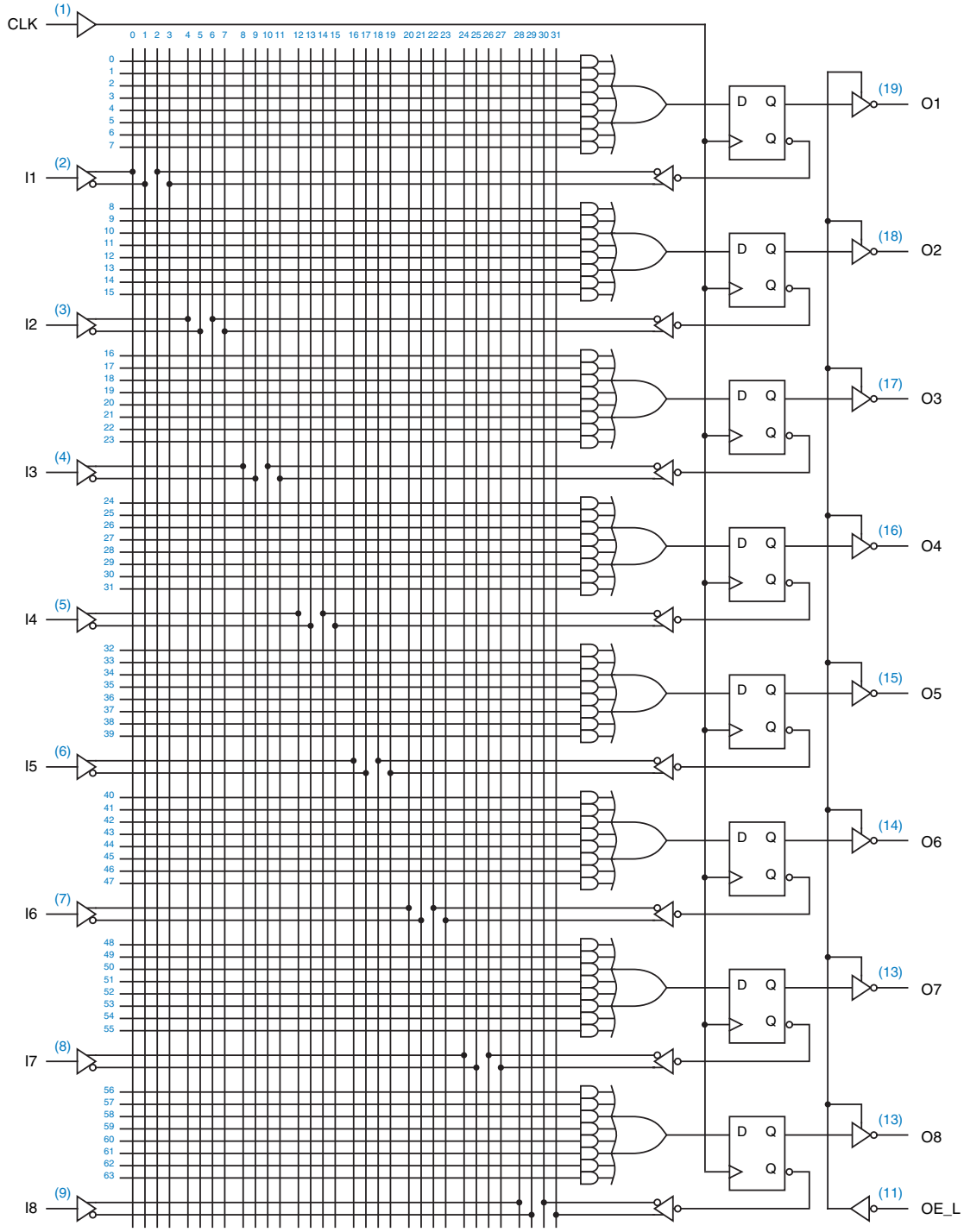

Figure BiPLD-2 PAL16R8 logic diagram.

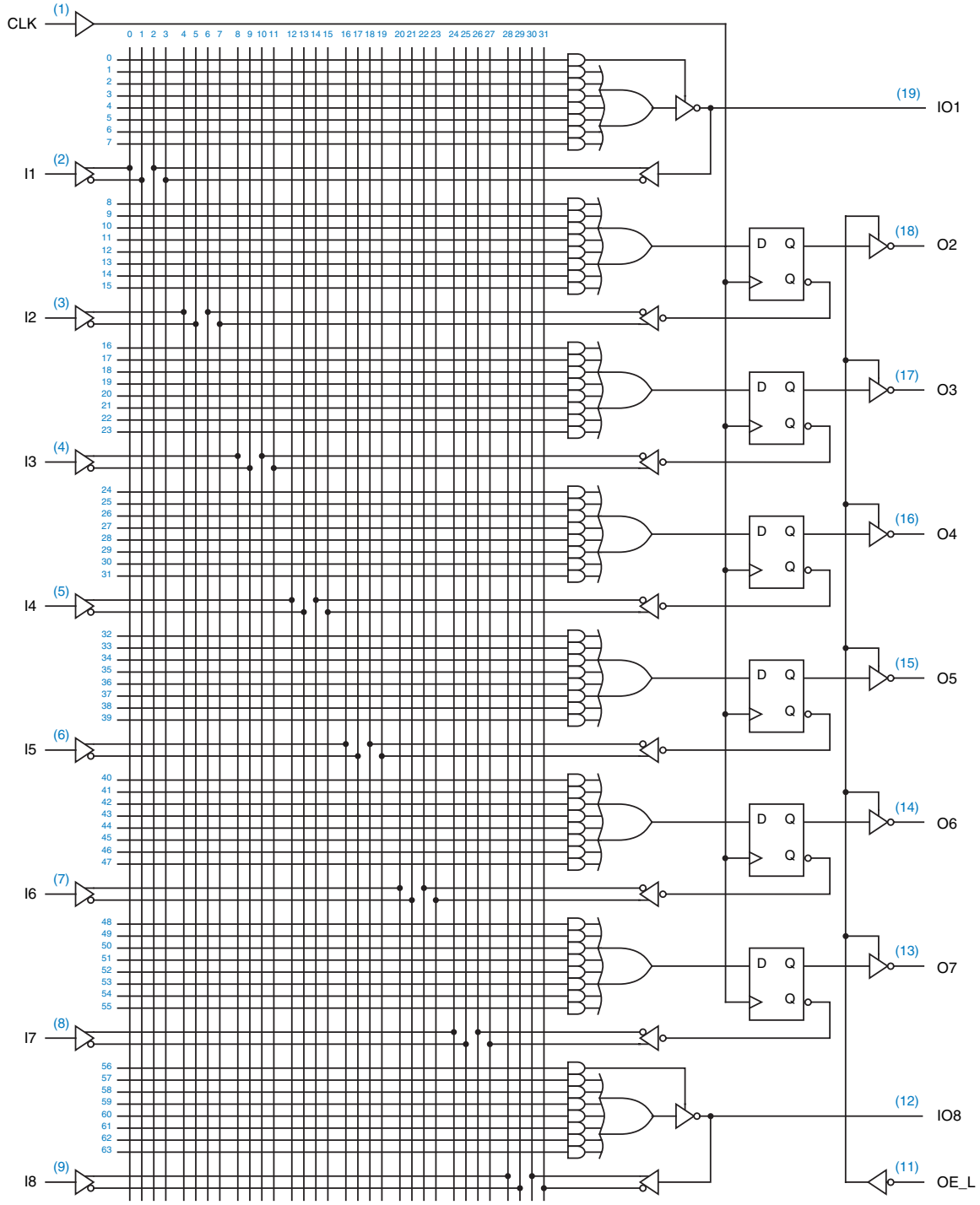

Figure BiPLD-3 PAL16R6 logic diagram.

Table BiPLD-1 Characteristics of standard bipolar PLDs.

			Inputs to AND array			
Part number	*Package pins*	*AND-gate inputs*	*Primary inputs*	*Bidirectional combinational outputs*	*Registered outputs*	*Combinational outputs*
PAL16L8	20	16	10	6	0	2
PAL16R4	20	16	8	4	4	0
PAL16R6	20	16	8	2	6	0
PAL16R8	20	16	8	0	8	0
PAL20L8	24	20	14	6	0	2
PAL20R4	24	20	12	4	4	0
PAL20R6	24	20	12	2	6	0
PAL20R8	24	20	12	0	8	0

Exercises

BiPLD.1 Determine the number of fuses in each of the PAL devices in Table BiPLD-1.

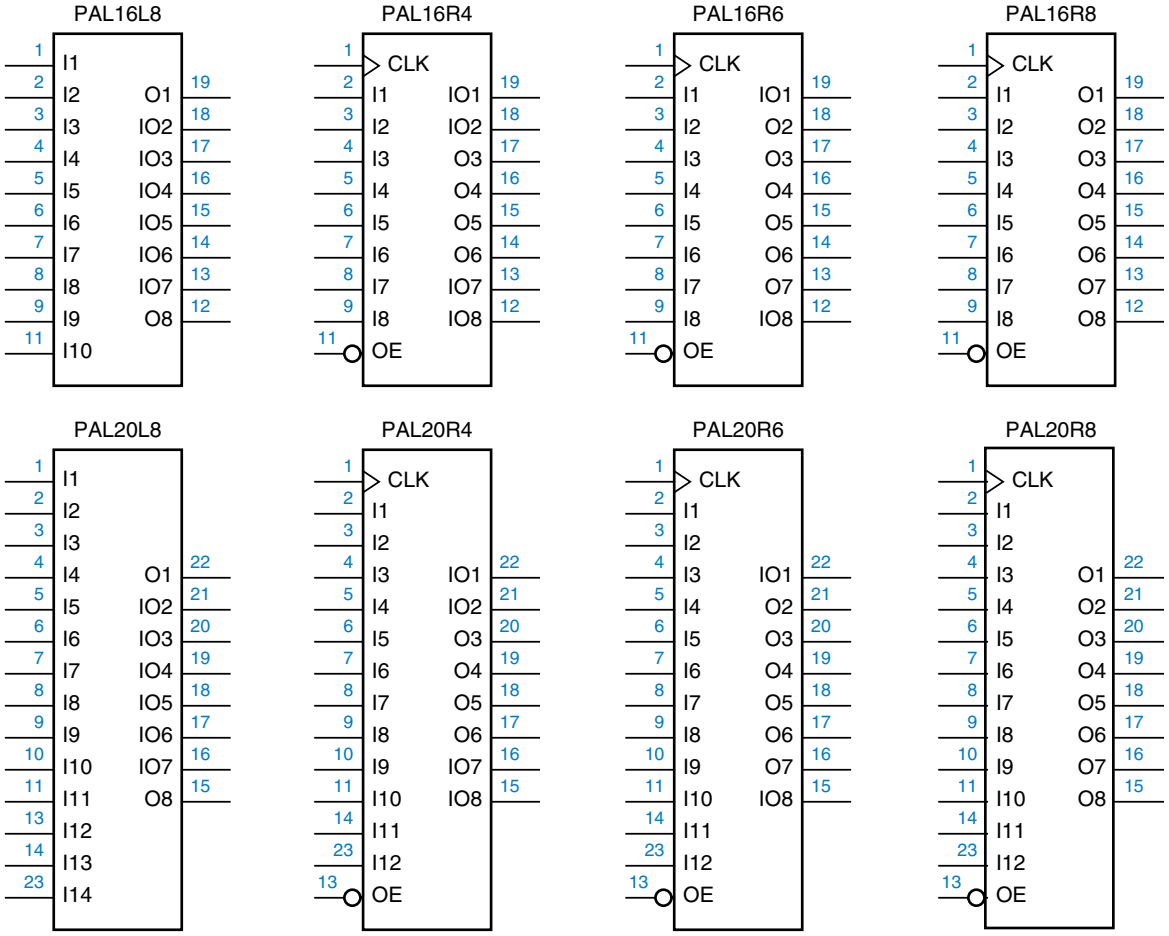

Figure BiPLD-4 Logic symbols for bipolar combinational and sequential PLDs.